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RECONFIGURABLE SYSTEM-ON-A-CHIP BASED PLATFORM FOR SATELLITE ON-BOARD COMPUTING

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Abstract: *This paper presents the results of an investigation into the suitability of advanced technologies to on-board applications. A generic single-chip computing platform for use on-board small spacecraft, which can be reconfigured remotely from the ground station, is proposed. The platform features a highly modular structure, such that it can be quickly and easily customised to produce specific-purpose controllers for data processing, communication and control of different spacecraft subsystems and payload blocks. Two schemes for on-board run-time partial reconfiguration are proposed, which will facilitate adding and updating of peripheral cores remotely (in space).*

1. Introduction

Small satellites aim to achieve low-cost, fast access to space and this is normally supported by the use of off-the-shelf components (COTS) and development tools. The advances in micro and nano technology, which have already brought to life remarkable new products and capabilities in terrestrial systems, are bound to change the way in which satellite on-board computing and electronics are designed.

Computing has always played an important role in on-board data processing and control. Historically on-board computing has been represented mainly by the on-board computer (OBC), which is the kernel of the On-Board Data Handling (OBDH) system that is central to the overall satellite design and its operations. The OBDH system is an integral part of the satellite platform and in many missions extends to comprise elements of payload electronics. Nowadays, a computer controls almost any single on-board sub-system and therefore on-board computing is represented by a number of computing units connected by an on-board data network. This is possible due to the emergence of advanced miniaturization technologies, which have given birth to multi-million system-on-a-chip (SoC) processor designs. This trend is going to be continued further and it is expected that in the near future all the electronics of a fully functional satellite will be condensed into one multi-chip module.

High-density programmable logic devices have become an established implementation medium in terrestrial systems, replacing application-specific integrated circuits (ASICs) in many applications due to lower cost, shorter time to market and hardware reconfigurability. Correspondingly, system-on-a-programmable-chip (SoPC) design has emerged as a major enabling technology. It is envisaged that the application of the SoPC concept to on-board computing will result in radical improvements and new capabilities. In addition to the traditional benefits of SoC design, such as reduction of size, complexity and cost, it can provide the means to build flexible and modifiable on-board computing systems.

This paper presents the results of an investigation into the suitability of advanced technologies, such as high-density SRAM-based Field Programmable Gate Arrays (FPGAs), system-on-a-chip design and reconfigurable computing to on-board applications. We propose a generic single-chip computing platform for use on-board small spacecraft, which can be reconfigured remotely from the ground station. This platform features a highly modular structure, such that it can be quickly and easily customised to produce specific purpose controllers for data processing, communication and control of different spacecraft subsystems and payload blocks.

The paper is structured as follows. Section 2 discusses the suitability of high-density FPGAs for SoC design. Section 3 outlines a generic reconfigurable SoC platfom for on-board computing. Section 4 is dedicated to on-board run-time partial reconfiguration.

2. System-on-a-Programmable-Chip Technology

The term "*system-on-a-chip*" defines both a product and a process [1]. As a product, SoC defines specific, targeted applications and contains an entire system. As a process, SoC defines system requirements that are modelled, analysed, and partitioned into hardware and software specifications for design and implementation.

The capacity and performance of FPGAs have been increasing steadily for more than a decade. Due to the rapid increase in transistor density FPGAs can now be employed as a platform for SoC implementation. Taking the Virtex series of Xilinx FPGAs as an example, the density increased from 1 M in 1998 to 15 M system gates at the end of 2004, as shown in Figure 1, with Virtex 4 FX series containing two embedded PowerPC processor cores [2, 3].

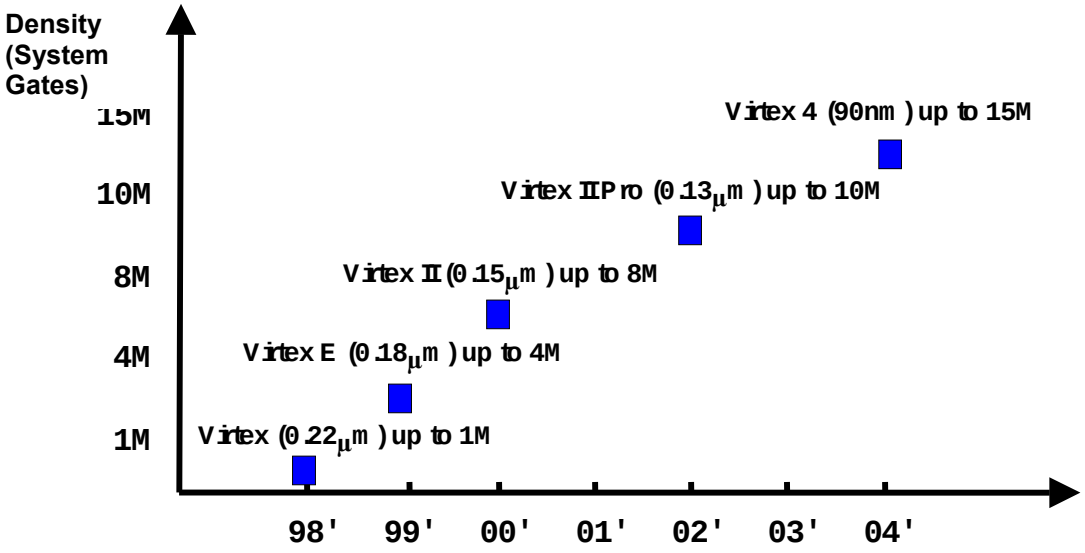

Figure 1. Density of the Xilinx Virtex Family of FPGA Devices

Intellectual Property (IP) cores are the building blocks of SoC designs. IP cores can be divided into three classes: soft, firm and hard cores [4]. Soft IP cores are generally offered in a synthesisable Register Transfer Level (RTL) description, which makes them inherently process-portable and reusable. However, soft IP cores must be re-implemented for each new SoC design. Re-implementation requires that the design goes through another iterative process of synthesis, floor planning, placement, routing, and back-end verification for each use.

An FPGA-based SoC platform offers many potential advantages, including low cost, very large scale integration, short time to market, and easy field upgrades of entire systems. A soft microprocessor IP core enables custom instructions and function units. The whole system can be reconfigured to enhance SoC development, debugging, testing, and tuning. All these benefits as well as the low cost of this approach make an FPGA-based SoC a promising solution for advanced on-board applications.

3. Generic Reconfigurable System-on-a-Chip Computing Platform for On-Board Applications

Performance requirements for space-flight electronics are increasing as on-board sensors produce greater amounts of data at higher resolutions [5]. A modular, reconfigurable and highly integrated SoC platform for on-board data processing, control and communication is a practical way to address some of these issues.

The proposed on-board SoC computing platform is based on soft IP cores and is targeted at high density reconfigurable FPGAs as the implementation technology. These features support increased system flexibility. The underpinning architectural principle of the SoC platform is modularity, which enables addition/replacement of blocks. This modularity is supported by an appropriate on-chip bus structure and unified interface of peripheral modules. At the hardware level, the SoC components can be classified from four different view points, as illustrated in Figure 2.

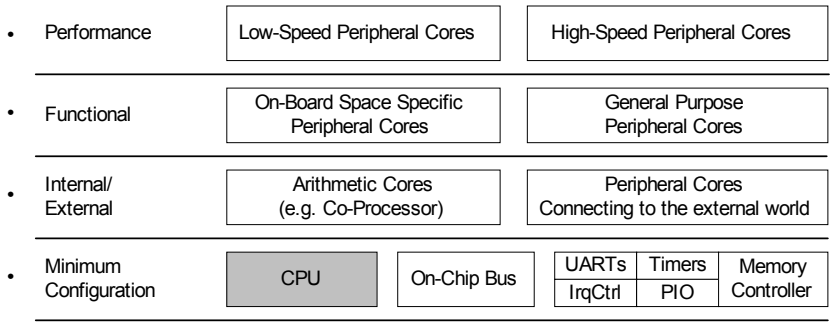

Figure 2. Conceptual Classification of SoC IP Components [6]

The SoC peripheral components can be divided into two groups according to their relationship with the external world. Arithmetic IP cores e.g. co-processor, encoder/decoder are internal blocks. External peripheral IP cores e.g. Controller Area Network (CAN) controller, High-level Data Link Control (HDLC) controller connect to board-level components and need that the corresponding FPGA I/O pins are programmable for the required standard voltage. In terms of function, the SoC peripherals can be specific to the space application, e.g. error detection and correction module (EDAC), triple modular redundancy (TMR) block, etc. or general-purpose cores, e.g. DMA controller. Furthermore, based on the performance, the SoC peripheral cores can be divided into high-speed and low-speed cores connecting to on-chip buses with different bandwidth.

The LEON processor IP core is selected as the central processing unit (CPU) for the platform. The LEON core, developed by ESA [7], is a synthesisable IP core written in VHDL, which is based on the SPARC V8 architecture. LEON-1 is the first version of the LEON VHDL model released in October 1999. The LEON-2 processor model [8] has two versions: standard and fault-tolerant (LEON-2FT) in which flip-flops are protected by TMR and all internal and external memories are protected by EDAC or parity bits. Recently, Gaisler Research released the LEON-3 model [9] with an improved pipeline and multi-processor support. The Microcontroller Bus Architecture (AMBA) bus [10], which is

supported by the LEON processor, is chosen as the on-chip bus for the SoC platform. It facilitates "right-first-time" development of embedded processors with one or more CPU/signal processors and multiple peripherals. The AMBA bus enhances the reusable design methodology by defining a common backbone for SoC modules.

The radiation tolerant QPro series of XILINX Virtex FPGAs were selected as the implementation medium for the SoC platform as they satisfy best the requirements of the platform architecture among the currently available FPGA devices. Experimental results have shown that the largest capacity device in the QPro family of up to 6 M system gates is sufficient for the SoC design implementation [13]. The QPro Virtex family are sensitive to single event upsets (SEUs) in space although they have a relatively good total dose resistance. Extensive testing of the sensitivity of Virtex devices to SEUs is carried out by the manufacturer and collaborators. Mitigation techniques that can correct the effects of the SEUs, such as triple modular redundancy, partial run-time reconfiguration and scrubbing are detailed in the literature [11].

The SoC platform can be configured to meet different mission requirements. Figure 3 illustrates an example configuration of the SoC platform architecture for a credit-card size on-board computer system with dimensions 85 mm × 54 mm and mass about 50 g [12]. The SoC on-board computer (SoC-OBC) consists entirely of soft IP cores including the LEON-2 processor and peripheral devices. A purpose-built Direct Memory Access (DMA) controller handles the data transfers between the peripheral cores and the main memory. The CAN, HDLC, SpaceWire interface controllers and the EDAC block are typical components and interfaces for use in space. The AMBA AHB bus is for interfacing of high-performance system modules. The AMBA APB bus supports peripheral functions with minimal power consumption and reduced interface complexity.

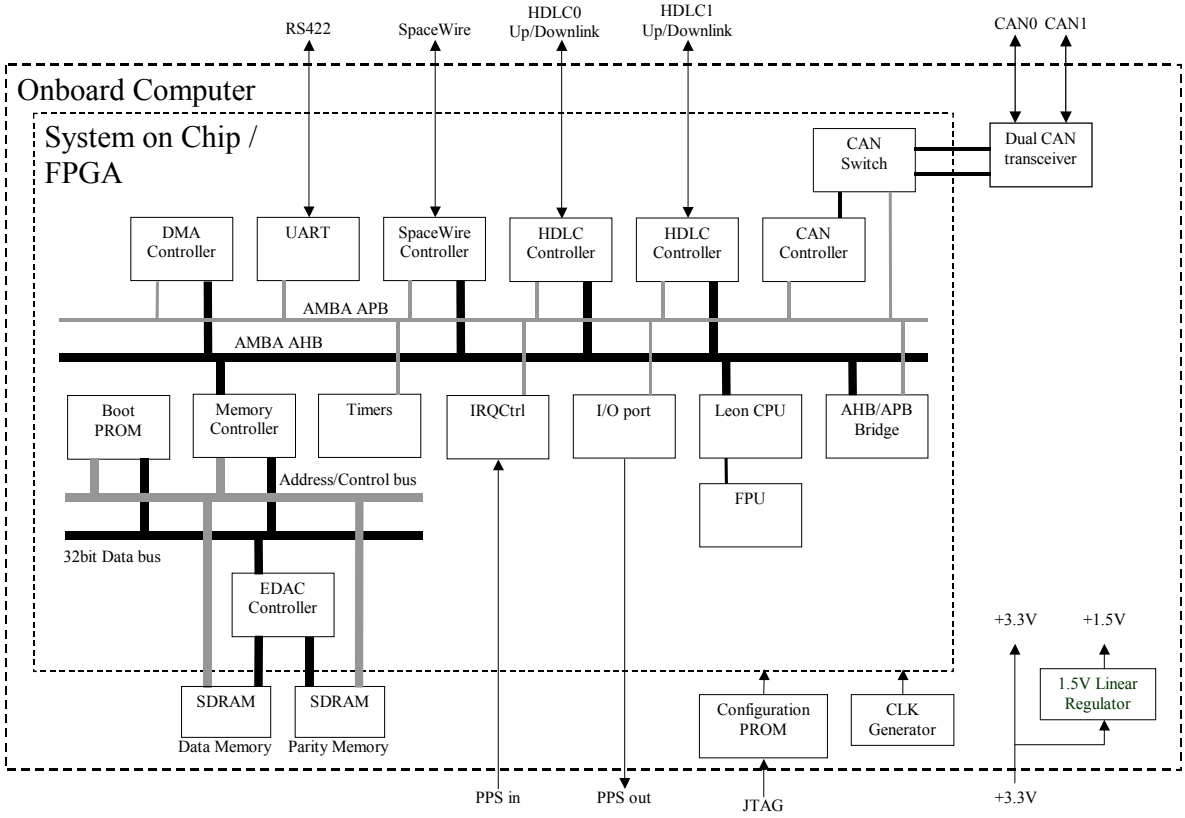

Figure 3. Example SoC-OBC Block Diagram

The standard version of the LEON-2 processor core was used in a proof-of-concept case study, as a result of which a downsized version of a SoC-OBC was implemented and tested with a software communication system [13].

4. On-Board Partial Run-Time Reconfiguration

Partial run-time reconfiguration (RTR) is the ability to update only a portion of the configuration memory in an FPGA with a new partial configuration without interrupting the functionality of the unchanged section of the FPGA. In the case of FPGAs, soft and firm cores are represented by bitstream files, which are generated at the last design stage and are ready to be used to configure the FPGA.

JBits is a set of Java classes developed by Xilinx, which provide Application Program Interface (APIs) into the Xilinx FPGA bitstream [14]. The APIs provide the lowest level interface to the Virtex architecture. This interface operates either on bitstreams generated by design tools, or on bitstreams read back from actual hardware, which can provide the capability of designing, modifying and dynamically modifying the logic on an FPGA. JBits gives the possibility to manually place, route and reconfigure an FPGA on a configurable logic block (CLB) level with relatively simple commands. This makes it very suitable for partial run-time reconfiguration. The power of using JBits is that it provides the ability to access both the regular logic and the configuration logic during the operation.

The traditional FPGA design flow cannot efficiently support RTR. A combined methodology is proposed that merges the traditional design approach with the JBits design flow. Two schemes for on-board partial RTR of the SoC-OBC are specified [6, 15]. The basic scheme is illustrated in Figure 4. The full bitstream for the complete SoC-OBC design and the partial bitstreams for every reconfigurable IP core are generated on ground. These bitstream files are downloaded in non-volatile on-board memory before the launch of the spacecraft. This scheme can be very useful for fault masking and SEU mitigation, but it can also be employed for updating of the SoC design. In case when one of the IP cores of the SoC-OBC needs to be updated or it is necessary to add a new IP core to the SoC-OBC a new partial bitstream file should be uploaded through the uplink. A configuration controller implemented in a radiation hardened FPGA or by a microcontroller handles the full and partial configuration of the Virtex FPGA on-board. A fallback situation, when the whole OBC needs to be reprogrammed and reset under some extreme circumstances (i.e. the processor core is dead because of SEUs), is also dealt with.

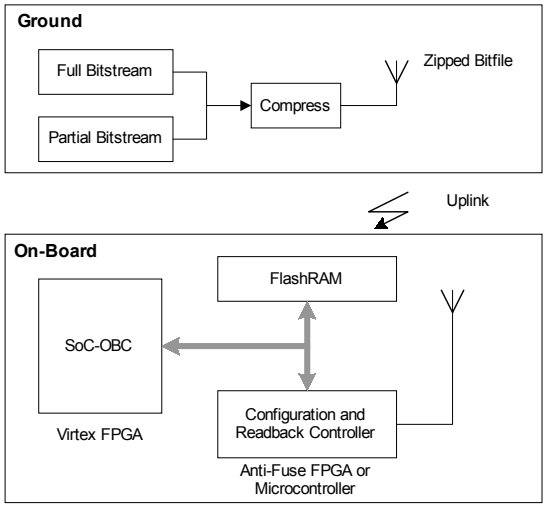

Figure 4. Partial Run-Time Reconfiguration of the SoC-OBC – Basic Scheme

The SoC-OBC can be partially run-time reconfigured in a remote way via Internet protocols (TCP/IP) using a client-server scheme. In this scheme, the partial RTR is achieved by integrating the JBits software and the Xilinx hardware interface (XHWIF) API. The SoC-OBC can be accessed via any TCP/IP network using the remote access capability of the XHWIF interface. When porting a SoC-OBC board to the XHWIF, the Java native interface (JNI) is employed to implement the board description code (in Java) and the system dependent functions providing access to the hardware (native methods in C). The SoC-OBC acts as an equivalent to an application server, allowing client Java programs to run on the server and use its resource for hardware reconfiguration, providing local (on-board) and remote access (from the ground).

5. Conclusions

In this paper we have described a generic system-on-a-chip platform for computing on-board small satellites, which can be partially reconfigured at run-time. This platform is targeted at the QPro radiation tolerant family of Xilinx Virtex FPGAs. It is composed of reusable soft IP cores and is centred on the LEON microprocessor core and the AMBA on-chip bus. Two schemes for on-board run-time reconfiguration are proposed, which can enable adding and updating of peripheral cores remotely (in space), while the rest of the OBC is operational.

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